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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,188	11/29/2000	Jari A. Parviainen	872.0025USU	5987

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,188	PARVIAINEN, JARI A.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/00;1/1/01;3/14/01;3/5/01;4/9/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6-7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 6-11, 15-18, 20-22, and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Matsuo et al. (U.S. 5,301,137) in view of Aldrich et al. (U.S. 6,601,077).

Re claim 1, Matsuo et al. disclose in Figure 1 a data processor comprising: a multiplier block (103) having a multiplier front end (output of 103) for generating partial products from input operands (101 and 102), and a plurality of arithmetic logic units (106) having inputs switchably coupled (108), in a first mode of operation (summing all the partial products from 103), to first data sources (output of 103) comprised of outputs of multiplier front end for adding together partial products received therefrom to arrive at a multiplication result (summing all the partial products from 103 through 107), inputs of plurality of ALUs being switchably coupled (108), in a second mode of operation (e.g. adding 101 and 102; col. 2 lines 55-59), to second data sources (101 and 102) for performing at least one of arithmetic and logical operations on data received from second data sources (col. 2 lines 55-59). Matsuo et al. do not disclose explicitly in Figure 1 a plurality of ALUs. However, Aldrich et al. disclose in Figure 3 an ALU (165) composes of several small ALUs (378 and 380). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a plurality of ALUs as seen in Aldrich et al.'s invention into Matsuo et al.'s invention because it would enable to reduce the hardware complexity and handle efficiently any size of data (col. 2 lines 1-3 and col. 2 lines 35-40).

Re claim 2, Matsuo et al. inherently disclose partial products have a width of n-bits, and where a width of ALUs is one of n-bits or less than n-bits (when there is more

than one sub ALUs in the ALU 106, each width of sub ALU must be equal or less than the width of ALU).

Re claim 6, Matsuo et al. do not disclose partial products have a width of n-bits, where a width of ALUs is less than n-bits, and where at least some of plurality of ALUs are switchably coupled together to provide an n-bit wide ALU. However, Aldrich et al. disclose in Figure 3 an ALU (165) composes of several small ALUs (378 and 380) and coupled together to provide an n-bit wide ALU (165). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a plurality of ALUs coupled together to form an ALU of n-bit wide as seen in Aldrich et al.'s invention into Matsuo et al.'s invention because it would enable to reduce the hardware complexity and handle efficiently any size of data (col. 2 lines 1-3 and col. 2 lines 35-40).

Re claim 7, Matsuo et al. further disclose in Figure 1 inputs of ALUs are switchably coupled under control of a program instruction (108).

Re claim 8, Matsuo et al. further disclose in Figure 1 plurality of ALUs, when in the second mode of operation, operate in parallel with one another on data (101 and 102) received from second data sources.

Re claim 9, Matsuo et al. do not disclose data processor forms a part of a wireless terminal. However, Aldrich et al. disclose in column 1 lines 15-18 the data processor forms a part of a wireless terminal (col. 1 line 17). Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add the data processor into a wireless terminal as seen in Aldrich et al.'s

invention into Matsuo et al.'s invention because it would enable to reduce the hardware, reduce the cost of implement, and increase the reliability in DSP in wireless communication (col. 1 lines 15-22).

Re claim 10, it is a method claim of claim 1. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 11, it is a method claim of claim 2. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 15, it is a method claim of claim 6. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 16, it is a method claim of claim 7. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 17, it is a method claim of claim 8. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 18, it is a method claim of claim 9. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 20, Matsuo et al. further disclose a reconfigurable signal routing logic (104 and 105) for providing data paths to and from plurality of ALUs.

Re claim 21, it is a DSP claim of claim 2. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 22, it is a DSP claim of claim 9. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 24, it is a DSP claim of claim 20. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 20.

6. Claims 3-5, 12-14, 19, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Matsuo et al. (U.S. 5,301,137) in view of Aldrich et al. (U.S. 6,601,077), as applied to claim 1, in further view of Cheung et al. (U.S. 6,369,610).

Re claims 3-5, Matsuo et al. in view of Aldrich et al. do not disclose implicitly partial products have a width of 8-bits/16-bits/32-bits, and where a width of ALUs is one of 8-bits or 4-bits; 16-bits, 8-bits or 4-bits; and 32-bits, 16-bits, 8-bits or 4-bits respectively. However, Cheung et al. disclose in Figure 6 a multiplier comprising a basic block of 4-bit ALU (Figure 6). In addition, 8-bit ALUs and 16-bit ALUs are multiple of Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add 4-bit ALUs as a basic function block into a multiplier as seen in Cheung et al.'s invention into Matsuo et al. in view of Aldrich et al.'s invention because it would enable to reduce the circuitry and simplify the complexity of hardware.

Re claims 12-14, they are method claim of claims 3-5 respectively. Thus, claims 12-14 are also rejected under the same rationale in the rejection of rejected claims 3-5 respectfully.

Re claim 19, Matsuo et al. in view of Aldrich et al. do not disclose implicitly a plurality of ALUs comprise the same or additional ALUs that are coupled to inputs of multiplier front end for changing a sign of input operands. However, Cheung et al.

disclose in Figure 4 that the operation of a multiplier of unsigned operands uses 2's complement for changing a sign of input operands (invert all bits +1). Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to change a sign of input operands as seen in Cheung et al.'s invention into Matsuo et al. in view of Aldrich et al.'s invention because it would enable the multiplier system to perform in signed operands.

Re claim 23, it is a DSP claim of claim 19. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 19.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,369,610 to Cheung et al. disclose a reconfigurable multiplier array.

b. U.S. Patent No. 6,574,651 to Cui et al. disclose a method and apparatus for arithmetic operation on vectored data.

c. U.S. Patent No. 5,570,039 to Oswald et al. disclose a programmable function unit as parallel multiplier cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

November 12, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100